REMARKS

This paper is timely-filed in response to the official action dated July 3, 2006.

Claims 1-3, 5-9, 11, and 12 are pending and at issue in this application. All claims 1-3, 5-9, 11, and 12 currently stand rejected under 35 U.S.C. §103(a) as obvious over admitted prior art in view of U.S. Patent Publication No. 2005/0032382 to Rossman ("Rossman").

By the foregoing, claims 1, 3, 6, 8, and 9 have been amended for clarity. Support for the amendments to claims 1 and 6 may generally be found throughout the application as filed. More specifically, support may be found at paragraphs 36 and 41. The amendments to claims 3, 8, and 9 merely address matters of form raised by the amendments to claims 1 and 3.

The sole basis for the claim rejections is addressed below. Reconsideration of the application, in view of the foregoing amendments and the following remarks, is solicited.

CLAIM REJECTIONS – 35 U.S.C. §103(a)

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. §103(a) as obvious over admitted prior art in view of Rossman. The Applicant respectfully traverses the rejections as applied to claims 1-3, 5-9, 11, and 12, as presented herein.

A *prima facie* case of obviousness must satisfy three legal requirements. First, there must be some suggestion or motivation, either in the references themselves, or in knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. *See* M.P.E.P. §2143. These criteria have not been satisfied with respect to claims 1-3, 5-9, 11, and 12, as explained in more detail below.

A. Independent Claim 1 and Dependent Claims 2, 3, 5, and 11

Claim 1 recites a method of manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate in which a gate electrode pattern is formed and forming an interlayer insulating film including a multi-layered oxide film by performing multiple simultaneous deposition-and-etch processes in order to bury the gate electrode pattern, wherein a ratio of deposition rate to etch rate is varied for each of the multiple deposition-and-etch processes, and the last deposition-and-etch process has a lower ratio of deposition rate to etch rate relative to the preceding deposition-and-etch process.

Rossman discloses a method and apparatus for increasing the deposition rate of a conformal dielectric layer. *See* Rossman at paragraph [0001]. Referring to claim 53 of Rossman, a deposition-to-etch ratio of a first deposition-to-etch process is decreased, and thereafter a second deposition-to-etch process is conducted with an increased deposition-to-etch ratio. Thus, in contrast to the method recited by claim 1, the last deposition-to-etch process has a *higher* ratio of deposition rate to etch rate relative to the preceding deposition-and-etch process.

The present application teaches that it is desirable to conduct the last deposition-and-etch process with a lower ratio than that of the preceding deposition-and-etch process so as to increase the smoothness of the interlayer insulating film. *See* application at paragraph 41.

In view of the foregoing remarks, the Applicant submits that a *prima facie* case of obviousness has not been established. Accordingly, the rejections of claims 1-3, 5, and 11 as assertedly obvious over admitted prior art in view of Rossman should be withdrawn.

B. Independent Claim 6 and Dependent Claims 7-9 and 12

Claim 6 recites a method of manufacturing a semiconductor device, comprising the steps of providing a semiconductor substrate in which a gate electrode pattern is formed, forming a first HDP oxide film over the entire structure by performing a first deposition-and-etch process simultaneously, and forming a second HDP oxide film over the entire structure by performing a second deposition-and-etch process simultaneously, wherein the first deposition-and-etch process has a higher ratio of deposition rate to etch rate relative to the second deposition-and-etch process.

As generally discussed above, Rossman discloses a method and apparatus for increasing the deposition rate of a conformal dielectric layer wherein a deposition-to-etch ratio of a first deposition-to-etch process is decreased, and thereafter a second deposition-to-etch process is conducted with an increased deposition-to-etch ratio. Thus, in contrast to the method recited by claim 6, the first deposition-and-etch process has a *lower* ratio of deposition rate to etch rate relative to the second deposition-and-etch process. Such a method increases the smoothness of the interlayer insulating film, thereby obviating the need for a subsequent CMP process, as disclosed at paragraph 41 of the present application.

In view of the foregoing remarks, the Applicant submits that a *prima facie* case of obviousness has not been established. Therefore, the rejections of claims 6-9 and 12 as assertedly obvious over admitted prior art in view of Rossman should be withdrawn.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance. Should the examiner wish to discuss the foregoing, or any matter of form or procedure in an effort to advance this application to allowance, he is respectfully invited to contact the undersigned attorney at the indicated telephone number.

Therefore, the Examiner is respectfully requested to pass this application to issue.

Respectfully submitted,

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